Collaboration

• Detectors & mechanical design: IPNO
• Embedded electronics
  – Si-strips & Si-Li / CsI boards: IPNO
• ASICs
  – 2 types: CEA & IPNO
• VXI, processing & acquisition: GANIL
Perspectives

- Improved dynamic range
- In-telecope ADC
- Fiber optics communication
- More channels (4-pi coverage)
- Pulse Shape Analysis
- ...

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VXI Board

- Bears the « remote side » of the detector (one daughter board / telescope)
  - Performs detector R/O and A to D conversion for all data types (Energy, timing, bias …)
  - Self-test, calibration and slow control
  - Trigger management
- Communication with DAQ
Si-Li & CsI board (MUSICA)

- Cascaded with MUFEE (same data link)
- No discriminator, no TAC
- Local peak-timing generation
Si-Li & CsI board (MUSICA)

- One single board for both detectors
  - 16 + 16 channels
- Single Asic type
  - Variable gain preamp (modularity 8?)
    - Si-Li = 250 MeV (Cf=10 pF)
    - CsI = 200 MeV (photodiode Cf=0.5 pF)
  - Shaper, T&H, Multiplexer, buffers
Si-strips board (MUFEE)

- Detector bias distribution
- 16 Asics w/ 16 inputs each
- E2PROM for local & private storage of the calibration parameters
- Calibration pulser
- Fast trigger / validation logic
- Analog and slow control interfaces
Si-strips ASIC (MATE)

- Data multiplexer & transmission buffer
  - Energy-Time
  - Bias current (on request)
- I2C slow control interface
- Fast trigger logic
Si-strips ASIC (MATE)

- 16 channels
- Dual polarity
- Each channel includes:
  - Preamplifier
  - Shaper
  - Track & hold
  - Leading-edge discriminator
  - TAC
  - Strip bias current measurement
System overview

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Technical Issues & Solutions

- Slow control, calibration and maintenance
  - One single, standard I2C link
  - Possible use of standard components
    - DACs, E2PROMS, temperature sensors ...

- Data transmission
  - High speed differential analog bus (2 MHz)
    - Common to all data types
Technical Issues & Solutions

- Volume and geometry
  - Extensive use of Asic technology
  - Early data multiplexing (in the telescope)
  - Robust data transmission and remote processing
- Power dissipation in vacuum
  - Minimize channel power $\rightarrow$ Asic
  - Dual board design with fluid cooling
Objectives

• Modularity
  – Easy future expansion
  – Easy replacement & repair

• Embedded intelligence
  – Self test
  – Calibration
MUST II: Objectives

- Provision for high channel count
  - 2 x 128 Si-strips + 16 SiLi +16 CsI / telescope

- Compacity
  - Small size embedded electronics
  - Low cable count

- Consistency
  - All detectors in one telescope connected to the same processing daughter board
MUST I

- VXI-D technology
- One VXI board for 120 Si-channels
- Discrete embedded preamplifiers
- Heavy wiring
  - One coax line for each Si-strip
- Custom designed trigger board
Outline

- MUST I
- MUST II
  - Motivations & Architecture description
  - Technology
    - The detector (embedded electronics)
    - The acquisition board
- Perspectives